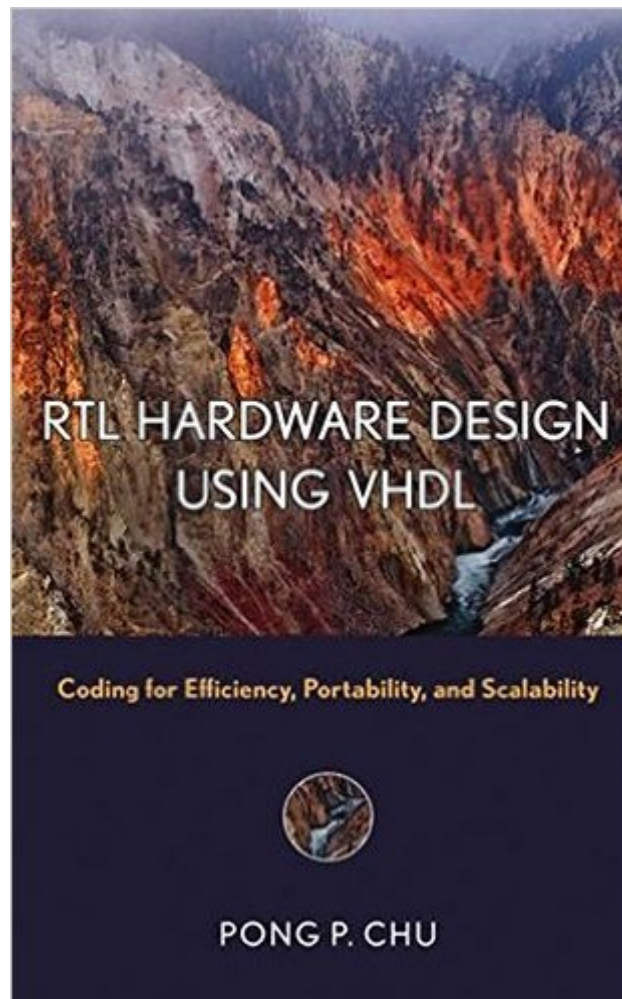


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# RTL Hardware Design Using VHDL: Coding For Efficiency, Portability, And Scalability



## Synopsis

The skills and guidance needed to master RTL hardware design. This book teaches readers how to systematically design efficient, portable, and scalable Register Transfer Level (RTL) digital circuits using the VHDL hardware description language and synthesis software. Focusing on the module-level design, which is composed of functional units, routing circuit, and storage, the book illustrates the relationship between the VHDL constructs and the underlying hardware components, and shows how to develop codes that faithfully reflect the module-level design and can be synthesized into efficient gate-level implementation. Several unique features distinguish the book:

- \* Coding style that shows a clear relationship between VHDL constructs and hardware components
- \* Conceptual diagrams that illustrate the realization of VHDL codes
- \* Emphasis on the code reuse
- \* Practical examples that demonstrate and reinforce design concepts, procedures, and techniques
- \* Two chapters on realizing sequential algorithms in hardware
- \* Two chapters on scalable and parameterized designs and coding
- \* One chapter covering the synchronization and interface between multiple clock domains

Although the focus of the book is RTL synthesis, it also examines the synthesis task from the perspective of the overall development process. Readers learn good design practices and guidelines to ensure that an RTL design can accommodate future simulation, verification, and testing needs, and can be easily incorporated into a larger system or reused. Discussion is independent of technology and can be applied to both ASIC and FPGA devices. With a balanced presentation of fundamentals and practical examples, this is an excellent textbook for upper-level undergraduate or graduate courses in advanced digital logic. Engineers who need to make effective use of today's synthesis software and FPGA devices should also refer to this book.

## Book Information

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## Customer Reviews

The world is well populated with books on elementary logic design, Katz's being one of the good ones. Such books present all the basics of hardware logic, registers, computer arithmetic, and maybe a little about a popular hardware description language (HDL), Verilog or VHDL. Then there are the language books that take basic logic concepts and show how to render them in one of the HDLs. Unfortunately, there's not much out there for the student who's mastered the basics, but isn't ready to dive in at the deep end of computer architecture. Chu's book meets the needs of that advancing student better than any other I know. After introductory chapters that orient the reader and set expectations, Chu dives in with a quick tour of VHDL basics. These 'basics', by the way, cover more detail than some entire texts. The next chapters cover principles and practice of combinational and sequential circuits, state machine design, register transfer level (RTL) design, and hierarchical design, with emphasis throughout on timing and efficient design. For example, sharing of functional units comes up as a topic in itself, something that arises in practice but rarely in the classroom. Toward the end, Chu presents the best discussion of parameterized design I've seen, including fairly advanced use of 'generate' statements and VHDL's alternative architectures. The last chapter covers design considerations for clock distribution and for crossing between clock domains, topics that arise in every non-trivial design and that continue to cause problems for designers. This book covers its topics better than any other I know.

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